CLAIMS

1. A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element both included in a package,

wherein an opening is formed in a center of a base provided with an input/output electrode pattern, the semiconductor integrated circuit is mounted in a center of an opening, and the semiconductor integrated circuit is connected to an electrode pattern on the base through a plurality of bumps.

2. The piezoelectric device according to claim 1, wherein the plurality of bumps formed on the semiconductor integrated circuit are formed at regular intervals on a center portion of an active element surface of the semiconductor integrated circuit.

3. The piezoelectric device according to claim 1, wherein the plurality of bumps formed on the semiconductor integrated circuit are concentrically formed about a center of an active element surface of the semiconductor integrated circuit.

4. The piezoelectric device according to claim 1, wherein a dummy bump is formed on an active element surface of the semiconductor integrated circuit.

5. The piezoelectric device according to claim 4, wherein the dummy bump formed on the semiconductor integrated circuit is connected to the electrode pattern on the base.

6. The piezoelectric device according to claim 1, further comprising a layered part, which surrounds the semiconductor integrated circuit, for mounting the piezoelectric resonator element, the layered part comprising at least two layers, including a first layer and a second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

7. The piezoelectric device according to claim 1, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4

to 0.45 times a length of a side of an opening in a pad provided on an active element surface of the semiconductor integrated circuit.

8. The piezoelectric device according to claim 1, wherein the base comprises a ceramic composite substrate.

9. The piezoelectric device according to claim 1, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is an Au bump.

10. The piezoelectric device according to claim 1, wherein a protrusion is formed in at least one side wall of the base facing the side of the semiconductor integrated circuit.

11. The piezoelectric device according to claim 10, wherein the protrusion is formed in each of side walls of the base facing two sides along the longitudinal direction of the semiconductor integrated circuit.

12. The piezoelectric device according to claim 10, wherein the protrusion formed in the side wall of the base has a substantially same height as, or is higher than, the semiconductor integrated circuit.

13. The piezoelectric device according to claim 10, wherein a gap between the protrusion formed in the side wall of the base and the semiconductor integrated circuit is set to a range between 0.05 and 0.15 mm.

14. A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element included in a package,

wherein an opening is formed in the center of a base provided with an input/output electrode pattern, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit is mounted in an opening, and the semiconductor integrated circuit is connected to an electrode pattern of the base through the plurality of bumps.

15. The piezoelectric device according to claim 14, wherein the plurality of bumps formed on the semiconductor integrated circuit are formed at regular

intervals at a center portion of the active element surface of the semiconductor integrated circuit.

16. The piezoelectric device according to claim 14, wherein a dummy bump is formed on the active element surface of the semiconductor integrated circuit.

17. The piezoelectric device according to claim 16, wherein the dummy bump formed on the semiconductor integrated circuit is connected to the electrode pattern on the base.

18. The piezoelectric device according to claim 14, further comprising a layered part on which the piezoelectric resonator element is mounted and which surrounds the semiconductor integrated circuit, the layered part comprising at least two layers including a first layer and a second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

19. The piezoelectric device according to claim 14, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

20. The piezoelectric device according to claim 14, wherein the base comprises a ceramic composite substrate.

21. The piezoelectric device according to claim 14, wherein the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

22. A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element included in a package,

wherein an opening is formed in the center of a base provided with an input/output electrode pattern, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit is mounted in a center of an opening, and the

semiconductor integrated circuit is connected to an electrode pattern through the plurality of bumps by ultrasonic bonding means.

23. The piezoelectric device according to claim 22, wherein a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit is perpendicular to two opposing sides of the active element surface of the semiconductor integrated circuit at which the plurality of bumps are formed.

24. The piezoelectric device according to claim 22, wherein a printing direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

25. The piezoelectric device according to claim 22, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

26. The piezoelectric device according to claim 25, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one being 80 to 90 μm in diameter and 30 to 35 μm in height, and the other being 40 to 45 μm in diameter and 30 to 35 μm in height.

27. The piezoelectric device according to claim 22, wherein the base comprises a ceramic composite substrate.

28. The piezoelectric device according to claim 22, wherein the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

29. The piezoelectric device according to claim 22, wherein a longitudinal direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

30. The piezoelectric device according to claim 22, comprising the semiconductor integrated circuit and the piezoelectric resonator element in included in the package,

wherein a vibration direction of ultrasonic waves for ultrasonic bonding and for forming bumps on the semiconductor integrated circuit and a vibration direction of ultrasonic waves for performing ultrasonic bonding of the semiconductor integrated circuit to the package are different from each other.

31. A method for manufacturing a piezoelectric device comprising a semiconductor integrated circuit and a piezoelectric resonator element included in a package, the method comprising:

a step of forming a metallic bump on the semiconductor integrated circuit;

a step of connecting the semiconductor integrated circuit on which the metallic bump is formed to a base by ultrasonic bonding;

a step of detecting a height direction of the semiconductor integrated circuit during the ultrasonic bonding;

a step of mounting the piezoelectric resonator element; and

a step of hermetically sealing a metallic lid to the base.

32. A method for manufacturing a piezoelectric device comprising a semiconductor integrated circuit and a piezoelectric resonator element included in a package, the method comprising:

a step of forming a metallic bump on the semiconductor integrated circuit;

a step of connecting the semiconductor integrated circuit on which metallic bump is formed to a base by ultrasonic bonding;

a step of detecting a height direction of the semiconductor integrated circuit during the ultrasonic bonding step;

a step of filling an underfill material around the semiconductor integrated circuit so as to cover an entire semiconductor integrated circuit including a rear surface of the semiconductor integrated circuit;

a step of mounting the piezoelectric resonator element; and

a step of hermetically sealing a metallic lid to the base.